REMARKS/ARGUMENTS

No claims are amended, canceled, or added. Thus, claims 1-22 remain pending.

Rejection under 35 USC 102(e), Wallace

Claims 1, 9, 10, 12, 14 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Wallace (US PG Pub 2006/0117280) (hereinafter Wallace_pub), which is a continuation of U.S. Patent No. 7,020,855 (hereinafter Wallace). As Wallace_pub was published after the filing date of the present application, 35 U.S.C. § 102(e) does not apply. Thus, Wallace is the appropriate reference and will be discussed hereafter.

Claim 1 is allowable as Wallace does not disclose or suggest each and every element of claim 1. For example, claim 1 recites:

> *selecting first and second LUTs from the design;*
> *determining whether both of the LUTs implement a same function; and*
> *if the first and the second LUTs implement the same function, combining masks of the LUTs into a shared LUT mask in the design.*

The current Office Action asserts that a logic gate is equivalent to a LUT. *See Office Action*, paragraph 31. As justification, the Office Action points to paragraph 3 of the present application. However, the appropriate passage is quoted incorrectly. In relevant part, paragraph 3 recites that a "lookup table (LUT) is a small binary memory circuit." *See present application*, paragraph 3. The current Office Action neglected to include the term "memory." Wallace only mentions a memory circuit 1104 in relation to the computer system that performs the calculation. *See Wallace*, Fig. 11 and col. 17 lines 3-30. Memory 1104 is not part of the "programmable integrated circuit" for which the design is being calculated, and Wallace does not mention a LUT or other memory circuit within the circuit being designed. Accordingly, Wallace does not teach or suggest the above limitations involving a LUT.

Additionally, the Office Action asserts that Wallace's discussion of merging [i.e. combining] two functions that implement the same functionality in conjunction with Wallace's discussion of placing schematics into layouts for circuit implementation [i.e. mask design] is

enough to suggest: "*combining masks of the LUTs into a shared LUT mask in the design*." *See Office Action*, paragraph 33.

Wallace states that "[m]erging of adjacent nodes may be controlled as follows. If two functions are the same function from {AND, OR, XOR) and one of them is an input to the other, the two functions are merged into a larger function." *Id.*, col. 9 lines 64-67 (emphasis added). As the merging creates a larger function, the two nodes do not share a mask. This is explainable in that Wallace's merging is not done at a physical level, but done conceptually for ease of analysis of swap structures. *Id.*, col. 9 lines 12-15 and col. 10 lines 24-32. For example, the resulting larger function would still utilize two separate AND gates to get a 3 input AND function. Whereas paragraph 21 of the present specification states "two look up tables (LUTs) in a design for a programmable integrated circuit can be combined into one shared LUT mask (SLM) to increase logic efficiency and to save area on the programmable IC." Accordingly, combining two AND gates to make a larger AND gate does not teach or suggest "*combining masks of the LUTs into a shared LUT mask in the design*." Also, note that no motivation is provided for the suggested combination.

For at least the reasons given, Applicant submits that claim 1 and its dependent claims 2-13 are allowable over Wallace. Applicants submit that independent claim 14 should be allowable for at least the same reasons as claim 1. Claims 15-22 depend from claim 14 and thus derive patentability at least therefrom.

Rejection under 35 USC 102, Wallace in view of Andreev

Claims 2-6, 11, and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace in view of Andreev et al. (6,848,094).

Claims 2-6 and 11 depend upon claim 1 and are allowable for at least the same rationale as claim 1. Claims 15-19 depend upon claim 14 and are allowable for at least the same rationale as claim 14.

Rejection under 35 USC 102, Wallace in view of Harrison

Claims 7, 8, 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace in view of Harrison.

Claims 7, 8, and 13 depend upon claim 1 and are allowable for at least the same rationale as claim 1. Claim 20 depends upon claim 14 and is allowable for at least the same rationale as claim 14.

In addition to being allowable for the same rationale as claim 1, claim 7 is allowable for additional reasons. For example, claim 7 recites:

> *before determining whether the LUTs implement the same function, determining if the LUTs have at least N common input signals; and if the LUTs do not have at least N common input signals, preventing the masks of the LUTs from being combined.*

The current Office Action asserts that Harrison teaches: determining the number of common or non-common inputs of two LUTs (i.e. at Fig 8 step 820, it is determined whether the LUT-implemented function block [see Col 16, lines 23-25 for "look-up table"] contains at least 21 inputs). *See Office Action*, paragraph 27.

In Harrison, step 820 examines a selected equation to determine if a single equation is FFB-OK, i.e. it can be implemented by a fast function block (FFB). *See Harrison*, col. 11 lines 31-56. By it own admission, the Office Action states that step 820 determines whether the equation contains at least 21 inputs. This characterization by the Office Action of only the inputs of one equation being examined is correct. However, since only one equation is being examined, Harrison does not teach or suggest determining common inputs of multiple equation, or even LUTS.

Since step 820 only evaluates on equation, Harrison does not teach or suggest common inputs between two equations, let alone identifying whether there are N common inputs. The only points where Harrison uses the term "common" is with reference to clock or enable signals, and not inputs of equations. *Id.*, col. 8 line 59 and col. 9 line 41. Additionally, there is not any description of the concept of common inputs between any two equations or subequations. Applicants thus respectfully request identification of where the concept of determining a number of common inputs is taught or suggested.

Furthermore, an equation is kept whole and not divided into two or more subequations if the number of inputs to the single equation is less than 21. *Id.*, col. 9 lines 58-60.

In contrast, two LUTs are kept in separate masks if the number of common inputs is less than N, as recited in claim 7.

For at least this additional reason, claim 7, and its dependent claim 8, are allowable over the cited references. Applicants submit that claims 13 and 20 are also allowable for at least the same reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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